Docket No.: 0104-0704P
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Michael O. THOMPSON et al.

Application No.: 10/088,913 Confirmation No.: 8909

Filed: May 7, 2002 Art Unit: 2824

For: NON-VOLATILE PASSIVE MATRIX DEVICE AND METHOD FOR READOUT OF THE SAME Examiner: J. H. Hur

RESPONSE TO USPTO COMMUNICATION DATED MAY 1, 2009

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Madam:

In response to the above noted USPTO communication regarding issues with the Appeal Brief, Appellants have addressed each of these issues in the concurrent filed Supplemental Appeal Brief.

Thus, Appellants respectfully submit that the Supplemental Appeal Brief is in compliance with 37 C.F.R . §41.37. Accordingly, entry of the Appeal Brief is respectfully submitted.

Please note, materials in Appendix D were previously provided with the Appeal Brief filed on June 24, 2008.

If the Examiner has any concerns regarding the Supplemental Appeal Brief, the Examiner is invited to contact Appellants representative Chad J. Billings, Reg. No. 48,917, at the number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Dated: May 29, 2009

Respectfully submitted,

By 

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Docket No.: 0104-0704PUS1
(PATENT)

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re Patent Application of: Michael O. THOMPSON et al.	**Before the Board of Appeals**
Application No.: 10/088,913	Confirmation No.: 8909
Filed: May 7, 2002	Art Unit: 2824
For: NON-VOLATILE PASSIVE MATRIX DEVICE AND METHOD FOR READOUT OF THE SAME	Examiner: J. H. HUR

SUPPLEMENTAL APPEAL BRIEF
IN RESPONSE TO PTO COMMUNICATION DATED MAY 1, 2009

MS Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

As required under § 41.37(a), this brief is being filed after the filing of the Notice of Appeal, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2), and any required petition for extension of time, if applicable, for filing this brief and fees related thereto, are dealt with in the accompanying TRANSMITTAL OF SUPPLEMENTAL APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1206:

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re Patent Application of: Michael O. THOMPSON et al.	**Before the Board of Appeals**
Application No.: 10/088,913	Confirmation No.: 8909
Filed: May 7, 2002	Art Unit: 2824
For: NON-VOLATILE PASSIVE MATRIX DEVICE AND METHOD FOR READOUT OF THE SAME	Examiner: J. H. HUR

SUPPLEMENAL APPEAL BRIEF ON BEHALF OF

APPELLANT: Michael O. THOMPSON et al.

MS Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I. REAL PARTY IN INTEREST

The real party in interest for this application is the Assignee, Thin Film Electronics ASA, P.O. Box 1872 Vika, N-0124 Oslo, Norway.

II. RELATED APPEALS AND/OR INTERFERENCES

There are no related appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-18 are currently pending in this application wherein claims 6-11 have been withdrawn from consideration. Claims 1, 12 and 13 are independent. The final Office Action

dated January 08, 2008 rejects claims 1, 13, 14, 16 and 17 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029) and Clemons (U.S. Pat. No. 4,599,709); claims 12, 15 and 18 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029), Clemons (U.S. Pat. No. 4,599,709) and Seyyedy (U.S. Pat. No. 5,969,380) and claims 2-5 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029), Clemons (U.S. Pat. No. 4,599,709) and Dierke (U.S. Pat. No. 5,734,615).

Claims 1-5 and 12-18 are the subject of the present appeal.

IV. STATUS OF AMENDMENTS

No further amendments have been presented after the outstanding Office Action of January 08, 2008.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

With respect to independent claim 1, the claimed invention is directed to a non-volatile passive matrix memory device in which the memory matrix which will allow for massive parallel readout at a high data rate with a reduction in the number of sense amplifiers ($26_1 - 26_k$) necessary for such a massive parallel readout. There is no limit to the number of bit lines, for example ($BL_1 - BL_k$) for each segment ($S_1 - S_q$) and therefore the memory matrix can be as large as necessary. The memory matrix is defined by a set of crossing word lines ($WL_1 - WL_m$) and a set of bit lines ($BL_1 - BL_k$). See figs. 5 and 6. A memory cell is defined in the memory material at the crossings between word lines and bit lines, wherein the memory cells of the memory device constitute the elements of a passive matrix. A passive memory requires each memory cell be at all times in physical ohmic contact with a word line and a bit line. See specification page 7, line 8 through page 9, line 35.

The word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line ($WL_1 - WL_m$) in a segment ($S_1 - S_q$) is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line ($BL_1 - BL_k$), where each separate bit line

assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means ($26_1 - 26_k$). This enables simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment. See specification pages 10 -11[1].

With respect to claim 12, the claimed invention is directed to a volumetric data storage apparatus, in which a plurality of stacked layers includes a non-volatile passive matrix memory device. The memory matrix allows for massive parallel readout at a high data rate with a reduction in the number of sense amplifiers ($26_1 - 26_k$) necessary for such a massive parallel readout. There is no limit to the number of bit lines and therefore the memory matrix can be as large as necessary. The memory matrix is defined by a set of crossing word lines and a set of bit lines (see figs. 5 and 6). A memory cell is defined in the memory material at the crossings between word lines ($WL_1 - WL_m$) and bit lines ($BL_1 - BL_k$), wherein the memory cells of the memory device constitute the elements of a passive matrix. A passive memory requires each memory cell be at all times in physical contact with a word line and a bit line. See specification page 7, line 8 through page 9, line 35.

The word lines ($WL_1 - WL_m$) are divided into a number of segments ($S_1 - S_q$), each segment including and being defined by a plurality of adjoining bit lines ($BL_1 - BL_k$) in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means ($26_1 - 26_k$), such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means. This enables simultaneous connection of all memory cells assigned to a

[1] *Specific reference to page 10 lines 15-21*

word line on a segment for readout via the corresponding bit lines of the segment. See specification pages 10 -11[2].

With respect to independent claim 13, the claimed invention is directed to a memory device, whereby the memory matrix allows for massive parallel readout at a high data rate with a reduction in the number of sense amplifiers necessary for such a massive parallel readout. There is no limit to the number of bit lines and therefore the memory matrix can be as large as necessary. The memory matrix is defined by a set of crossing word lines and a set of bit lines (see figs. 5 and 6). A memory cell is defined in the memory material at the crossings between word lines and bit lines, wherein the memory cells of the memory device constitute the elements of a passive matrix. A passive memory requires each memory cell be at all times in physical contact with a word line and a bit line. See specification page 7, line 8 through page 9, line 35.

The memory matrix is divided into a number of segments, each segment ($S_1 - S_q$) including and being defined by a plurality of adjoining bit lines ($BL_1 - BL_k$) in the matrix, each word line ($WL_1 - WL_m$) in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means ($26_1 - 26_k$). This enables simultaneous connection of all memory cells assigned to a word line on a segment. See specification pages 10 -11[3].

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[2] *Specific reference to page 10 lines 15-21*
[3] *Specific reference to page 10 lines 15-21*

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Final Office Action provides the following ground of rejection for review on appeal:

(a) Claims 1, 13, 14, 16 and 17 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029) and Clemons (U.S. Pat. No. 4,599,709);

(b) Claims 12, 15 and 18 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029), Clemons (U.S. Pat. No. 4,599,709) and Seyyedy (U.S. Pat. No. 5,969,380); and

(c) Claims 2-5 under 35 U.S.C. 103(a) in view of Kuroda (U.S. Pat. No. 5,487,029), Clemons (U.S. Pat. No. 4,599,709) and Dierke (U.S. Pat. No. 5,734,615)

VII. ARGUMENTS

A. The Rejections Fail to Establish *Prima Facie* Obviousness of Independent Claims 1, 12 and 13

1. Argument Summary

The Examiner's reasoning provided in support of the rejection of independent claims 1, 12, and 13 under 35 U.S.C. §103(a) as being obvious under the combination of *Kuroda* in view of *Clemons* and with respect to claim 12 *Seyyedy,* fails to establish *prima facie* obviousness. Specifically, the examiner has failed to provide references that teach or suggest all of the claim features. The Examiner has failed to provide references that refer to teaching of passive matrix memories and their characteristics. Instead, the Examiner provides references that teach active and other memories.

2. The Relied Upon References, Kuroda, Clemons and Seyyedy, Do Not Teach All the Claimed Elements Recited in the Independent Claims.

a. Difference Between Passive, Active and Other Memories

Appellants respectfully submit that the teachings of the applied references Kuroda, Clemons, and Seyyedy teach active memory devices or other types of memory devices all of which are entirely different from a passive matrix memory array of the claimed invention. These differences lead to a disconnect between the teachings of the references and the claimed elements. In illustrating this point, Appellants discuss the differences between the various types of memories in order to help point out the Examiner's error in applying each reference.

The present invention concerns a passive matrix-addressable ferroelectric or electret memory. This of course follows from the fact that the memory is an electrically polarizable dielectric material exhibiting hysteresis. Moreover the memory device according to the invention is a passive device, i.e. all the memory cells of the memory array is contacting the electrodes permanently. This contrasts with an active matrix-addressable memory, wherein each memory cell comprises a switching means, usually a FET transistor for establishing an electrical circuit between the memory cells and for instance its bit line electrode. This means that while all the memory cells of a passive matrix-addressable memory permanently are connected in an RC network, in an active matrix-addressable memory a memory cell selected for an addressing operation, i.e. a write or read operation, is switched into the network by switching means connected with a memory cell.

Both types of memory have their advantages and disadvantages. In a passive matrix-addressable memory a write or read operation consists in applying a switching voltage or potential over a selected memory cell and record a charge or current output response on the bit line by means a sense amplifier connected thereto. The so-called switching voltage which is applied for an addressing operation is usually selected much larger than their coercive voltage of the memory material. This implies that as an average a memory cell will be switched in 50% of the addressing operations, i.e. its polarization direction will be reversed. This amounts to a destruction of the

datum stored in the memory cell, such that for instance a stored logical 0 will be switched to a logical 1. In such cases a memory cell has to be reset by performing a writing operation and this is done by once more applying a switching voltage to the memory cell, but of the opposite sign. In a passive matrix-addressable memory an addressing scheme with destructive write and read sets up so-called sneak currents and disturb voltages in the permanent RC network formed by the memory cells of the array. This in addition to parasitic or stray capacitances that are bound to occur, and in sum these effects may either change the set polarization state of a memory cell and cause spurious output responses on the bit lines in a read operation.

As well known to persons skilled in the art the unfortunate effects of destructive write and read in a passive matrix addressable array is abated by for instance subjecting all addressing operations to a so-called voltage pulse protocol and the use of an appropriate voltage selection rule which will serve to minimize potential differences on unselected memory cells during an addressing operation.

The unfortunate effects in connection with the destructive write and read operation are avoided in active matrix-addressable memories, since only a selected memory cell is connected to a word line and a bit line. Usually such memory cells are termed 1T-1C memory cell, which denotes a memory cell with one switching transistor and one ferroelectric capacitor (for instance). Other configurations are known, e.g. memory cells of the type 2T-2C etc. The penalty of this is that the use of switching transistors in an active matrix tends to be power-consuming and moreover makes the memory array larger and more complicated. Also the number of electrode lines is doubled, as selection lines for the gate electrodes of the switching transistors will be needed and the data has to be output on a data line, which is joined to one memory cell electrode, i.e. one of the plates of the capacitor formed by the memory cell, upon switching the transistor channel to conduction. The data line is then for instance connected to the drain contact of the switching transistor. The bit line proper is then the electrode that connects one or more e.g. ferroelectric capacitors with the source contact of the switching transistor. It should furthermore be noted that even an active

matrix-addressable array is not completely free from parasitic capacitances, which by the way is a well-known problem in integrated circuit technology.

Generally ferroelectric memories have a much slower response than semiconductor memories such as DRAMs and SRAMs and hence the ferroelectric memories are better suited for use as ROM and WORM (Write Once, Read Many times). It should also be noted that in ferroelectric memories the data content cannot be erased, i.e. the memory cannot be set to a virgin state, but is non-volatile in the sense that a polarization state in principle could be maintained indefinitely and only completely erased by raising the temperature of the memory above the Curie temperature of the ferroelectric material, something which will return the material to its paraelectric phase. However, the fairly slow response of a ferroelectric memory can be offset by reading a large number of memory cells in parallel. In principle all memory cells on a word line can be read simultaneously, provided that each bit line is connected with a sense amplifier. Now there is also a penalty for this.

While ferroelectric memory arrays can be made extremely large, comprising millions or even hundred of millions of memory cells, it has turned out that it is difficult to operate a memory with more that 2000 word lines. In this case each bit line will be permanently connected in the passive configuration to no more than 2000 memory cells. One reason for this is the occurrence of floating charges on the bit line, a problem that aggravates with the number of memory cells on the bit line, and while it could be tempting to lower the access rate so that floating charges may decay, this would make the memory intolerably slow to operate. So the number of word lines is for practical reasons the typical ferroelectric memory material limited to about 2000, the exact number being dependent on the actual ferroelectric memory material used.

The capacity of memory can, however, be increased by resorting to a large number of bit lines, e.g. 16000 or 32000, which would respectively produce a memory array of 32 or 64 million memory cells. Performing a parallel readout of all memory cells on a word line in the latter case would imply that each bit line is connected with a sense amplifier, making 32000 sense amplifiers all told. It is easily seen that this would even with a slow response time of 1 μs yield a data rate

corresponding to 32 GHz. There are several reasons why this arrangement is not desirable. One is the problem of handling this data rate, the other is the very large number of sense amplifiers that is needed, and considering that a sense amplifier usually comprises two operation amplifiers, this implies at least 50 to 60 transistors for each sense amplifier. However, a more than adequate data rate would be 1 GHz, which would be competitive with fast DRAMs and SRAMs and would then, of course, imply parallel read of 1000 bit lines at once. Typically a data word read in this manner shall consist of 1 K bits or 128 bytes. By dividing the word line into segments of say 1024 memory cells a correspondingly large data word may be read in about 1 μs by connecting all the bit lines forming the word line segment to sense amplifiers. As a consequence a number of sense amplifiers can be reduced to the number of bit lines in a word line segment and with obvious advantages. This is precisely what the present invention discloses. Such an arrangement is not known in the prior art, and is neither anticipated nor suggested in any or the prior art documents cited by the Examiner.

Appellants have provided attachments[4] A/1 through D/11 which describe various types of memory architecture and provide the following discussion of each. Attachment A/1 discloses a conventional active ferroelectric memory as known in the art. Specifically it depicts a memory with four memory cells, each of which comprises a ferroelectric capacitor and a switching transistor. Hence the memory cells are of the type IT-IC. Memory cell types with more transistors and more capacitors are, however, known for instance a 2T-2C memory cell. Bit lines 314 are each connected with a sense amplifier, while two sets of word lines are used, namely those marked SWL which are used for gating the switching transistors of each memory cell 302 as well as driving word lines or pulsing word lines PWL connected both with a memory control logic as well as a source contact of additional switching transistor 315, one of which is provided for each pulsing word line. On accessing a memory cell the select word line SWL is pulsed high at the same time as the pulsing word line PWL connected with a memory control logic is also pulsed high. The word line switches 315 are of course jointly gated from the switching word line SWL and as a result the pulsing word

[4] *Attachments A/1 – D/11 are found in Appendix D*

line PWL goes high. The capacitor of the selected memory cell discharges through the now conducting switching transistor of the memory cell and to the bit line or data line 314, outputting a charge or current response from the selected memory cell to be sensed by the sense amplifier 206. The arrangement depicted in the enclosed figure 3a allows for a parallel readout on both memory cell collected to one and the same pulsing word line PWL, i.e. all memory cells in a row. As will also be seen, only the selected memory cells have their capacitors temporarily in ohmic contact with the electrodes. Hence no voltage disturb to the unselected memory cells are generated. Persons skilled in the art will furthermore realize and know that also the active matrix-addressable array in fig. 3a can be provided without parallel access, i.e. only a single memory cell can be selected at a time and brought into ohmic contact with the electrode. This shall however, necessitate an additional bit line or data line, one of which connects to the sense amplifier for readout.

Fig. 3b on sheet B/1 depicts a passive ferroelectric memory. Memory material of the memory cell indicated by 315 in fig. 3b is provided between word line electrodes 310 and bit line electrodes 314 where they cross to form a matrix of passive addressable memory cells formed in memory material between the crossing of electrodes 314 and 320. Note that the ferroelectric memory material, which is a dielectric, can be provided as a global layer between the electrodes 310 and 314. A ferroelectric capacitor is shown schematically in fig. 4, and 315 depicts the ferroelectric thin film interspersed between metal electrodes, e.g. word lines 310 and bit lines 314. As will be seen, the dielectric material, i.e. the ferroelectric material of the capacitor, is at all times in ohmic contact with the metal electrodes. The problem with this is that when a memory cell for instance as depicted at the crossing 320 is selected for write and read, a switching of the polarization of this memory cell shall cause a voltage disturb to all the remaining cell in the array, something which may result in floating capacitances on the bit line, spurious readout values and in the worst cases inadvertent switching of unselected memory cells, thus changing their polarization states and altering the logical values of the data stored. The ferroelectric material may be inorganic, typically a perovskite, or organic, typically a polymer or copolymer of vinylidene fluoride. Such a polymer spontaneously forms a diode junction to one of the

electrodes as depicted at 322, thus blocking a charge flow in an opposite direction. In case of an inorganic ferroelectric material a thin layer of a semiconductor, e.g. gallium arsenide, may be provided between the ferroelectric thin film and a metal electrode in order to create a Schottky diode junction.

A static random access memory is documented on attachments C/1-C/5 as downloaded from Wikipedia and herewith enclosed. This is the type of memory cell used in Clemons which explicitly is stated to be an SRAM. SRAMs are usually organized in CMOS architectures as depicted in the figure in C/2 and comprise six transistors, viz. 2 access transistors and 4 memory transistors in the form of two cross-coupled inverters M1-M4. They form the bistable latching circuit used to store a bit and the stored bit is retained by an SRAM as long as the memory circuit is powered. Hence no periodical refresh is required as is the case of a dynamic random access memory. Disturb of the memory cells is of course no issue here, but note that the configuration shown uses two bit lines, although it is possible to come away with only one. Two bit lines are, however, used as it will allow for differential signaling and highly improve the signal-to-noise ratio. Compared with both active ferroelectric memories and passive ferroelectric memories a SRAM has a much lower integration and consumes far more real estate, typically 6 times as much as a high density passive ferroelectric memory cell, in addition to also being more power consuming.

Attachments D/1 -D/11 show a true hybrid between a ferroelectric memory cell and conventional CMOS-based random access memories, namely a FERAM. As known by persons skilled in the art, a DRAM includes both signal transistors as well as capacitors and need to be continually refreshed. A SRAM memory cell has at least four storage transistors as well as two access transistors, while active matrix-addressable ferroelectric memories may have a memory cell with one access transistor or one storage capacitor.

Finally, we have the passive ferroelectric memory cell as used in the present invention. Both DRAM and FERAM use a capacitor and switching transistors of the memory cell proper. In both cases it is similar to that of the l T-1 C type and hence comparable to an active ferroelectric

memory. Both FERAM and an active ferroelectric memory differ from a DRAM as they similarly to the SRAM have no need for refresh (and the ferroelectric memory is of course truly non-volatile). The same of course also is valid for a passive ferroelectric memory. The big advantage of a FERAM seems to lie in the fact that it can be configured to be read non-destructively as apparent from D/1 to D/5. This is due to the fact that the direction of the remanent field of the ferroelectric capacitor which is provided as the gate insulator between a gate electrode and a transistor channel actually influence the source/drain current by affecting the movement of charges in the semiconductor substrate, i.e. speed and direction. This results in a different current output response from the transistor without the need for applying a switching potential across the ferroelectric material and between the gate electrode and the transistor channel. Writing, i. e. changing the polarization state of the FERAM must take place as with conventional ferroelectric memories, namely by applying a switching potential or not depending on whether the polarization state shall be changed or not in the writing process.

b. Teachings of Kuroda

The Examiner has provided Kuroda to teach the use of a passive matrix memory. The Examiner implies that blocks (1,1)...(1,7) shown in Fig. 1 provide a passive matrix memory array because each intersection of word and bit lines includes only a capacitor but no switching means. However, a passive matrix memory requires the ferroelectric material of the capacitor be at all the time are in ohmic contact with the metal electrodes. **Appellants recite this language explicitly within claims 1, 12 and 13 which is not taught by Kuroda.**

Kuroda does not teach this and in fact teaches to the contrary. First, nowhere does Kuroda teach or suggest that it provides a passive matrix memory. Further, nowhere does it teach characteristics that conform to a passive matrix memory. To the contrary a person skilled in the art would contemplate Kuroda and observe that the stated object in Kuroda is to improve on an active matrix-addressable memory by increasing its integration and by reducing the overall

voltage disturb, which Kuroda terms the voltage stress. The increased integration is achieved by instead of having for instance an IT-IC memory cell, resorting to a memory circuit with one switching transistor capable of switching memory cell, for instance shown as Q1, Q2, Q3 and so on. These memory circuits actually comprises 8 memory cells as depicted by their capacitors shown with one electrode connected via the source contact of the switching transistor Q1. In other words, Kuroda provides a true active memory circuit, and each capacitor of a circuit of course corresponds to a bit spot or a memory cell.

Further, it is a stated objective of Kuroda to appreciably reduce the voltage disturb as compared with a passive matrix-addressable memory cell. This is achieved by selecting a single memory circuit of a block, for instance block (1,0) in fig. 1, at a time and then selecting a single memory cell of this memory circuit for write and read to be preformed via a write/read control logic circuit WRCO with one sense amplifier SA and one write amplifier WA. The selection of a memory circuit takes place by pulsing the selection word line WB1 high and similarly setting either a data line DO, D1... high or a word line W10...W17 high with a resulting charge or current response from the memory cell connected to one of the word lines W10-W17 of each of the 8 memory cells of a memory circuit.

An X decoder XDEC and a Y decoder YDEC are provided in addition. All blocks of a column are connected via a multiplexer arrangement (YSELECT) with appropriate switching transistors Q4...Q9 and so on to the write/read control circuit WRC. This write/read control circuit WRC is moreover used to apply a voltage pulse protocol with a half voltage selection rule in order to further enhance the disturb strength of this memory. Table 1, col. 16-17 of Kuroda illustrates where Kuroda distinguishes between the memory of his invention and known prior art memories. In this table Prior Art 1 conforms to a wholly passive ferroelectric memory, i.e. with no switching elements at all and similar to the present invention, Prior Art 2 conforms to a fully active ferroelectric memory with cells of the I T-I C type and finally Prior Art 3 evidently to for instance a ferroelectric memory of the active type with memory cells for instance of the 1T-2C type and so on. The latest prior art could be seen as an advance towards

the approach taken by Kuroda, but differs essentially from Kuroda as Kuroda discloses the memory circuit with 8 capacitors and one switching transistor, thus with one capacitor for each memory cell. The main difference here is of course the blockwise arrangement of Kuroda which can be regarded as essential to achieving the desired low voltage disturb. As given at the bottom of column 17 and the top of column 18 of Kuroda, it is seen that his invention provides a disturb coefficient which can be given as 1.006. This is of course not much higher than the unity disturb coefficient of an active matrix-addressable array, while the disturb coefficient is in a passive matrix-addressable memory as used with the present invention is given as 1.025 and apparently correspondingly high in the configuration according to Prior Art 3. Relevant here is that with regard to disturb, Kuroda for all practical purposes is identical with the active matrix-addressable memory, but by reducing the number of switching transistors to 1/8 of the relevant prior art, he is able to achieve a correspondingly higher integration.

Thus, while the use of capacitors at the junction between a word and bit line in the bitewise arrangement of Fig. 1 appears in the doorway to represent a passive matrix memory architecture on the surface, the facts as disclosed by Kuroda suggest an active matrix memory. Thus, based on these facts one of ordinary skill would also presume that Kuroda teaches an active matrix memory and not use it for teaching a passive memory as claimed.

c. Teachings of Clemons

Clemons concerns a completely different kind of memory, namely a semiconductor memory of the SRAM type and a multi-bit organization. Clemons discloses how to achieve a memory architecture tailored to a bytewise organization by dividing the memory into block-like arrangement such that all bits of a byte accessed in a given operation are obtained from physically adjacent columns referred as byte blocks and thus distinguished above input/output blocks in prior art, see Clemons col. 4, lines 40-45. Clemons teaches nothing more than providing a bytewise-organized memory by defining blocks of the memory in terms of a bytewise arrangement made up of adjacent data lines such that, for instance, a byte may be read in parallel from one row of memory cells in a block at a time.

In consideration of the complexity of the various memory devices, Appellants have attached hereto a table[5] labeled as table 1 highlighting the differences between, Kuroda, Clemons, the alleged combination of Kuroda and Clemons as compared to the present invention.

3. One of Ordinary Skill Would Not Combine the Teachings of Clemons with Kuroda to Achieve Appellants Claimed Invention

a. Kuroda Does Not Teach or Suggest Parallel Read Out – One of Ordinary and of Common Sense in the Art Would Not Conclude it Obvious to Try to Force Parallel Readout on Kuroda's Memory by Combining it with Clemons Teachings

Kuroda does not allow for parallel readout. Only a single memory cell of a single circuit in one block of a column of blocks is read at a time. As already stated, the Y-SELECT block is used to multiplex the data lines to connect with the sense amplifier SA (or write amplifier WA) in the write/read control circuit WRC at the bottom of each column. In principle of course a parallel read could be obtained in Kuroda by allowing in the simultaneous reading of one memory cell in each block and on one and the same word line (row) via the single sense amplifier provided for each column. This would amount to reading an eight-bit byte in parallel, but would then nullify the expressly stated object of Kuroda to keep the voltage disturb or voltage stress coefficient low. Attempting parallel readout in this manner would actually *increase* the disturb coefficient by a factor of 8.

Kuroda discloses essentially a very small memory capable of storing only 1024 bits, but with very high integration factor. These memories could be realized with extremely small dimensions and should hence be eminently suited for the applications as indicated in Figs. 56-59, where they are shown provided in great numbers and distributed in respective technological systems such as automobiles, airplanes, space stations and rockets to handle measurement and control functions. Hence the low storage capacity is offset by being able

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[5] *Table 1 is found in Appendix D*

to provide one highly integrated memory chip for each function.

Moreover it is no doubt that the architecture and mode of operation envisaged by Kuroda, namely an access rate of one bit at a time from each memory, shall to a high degree serve to contribute their reliability in the applications as envisaged and illustrated in Kuroda. Such desirable properties would however, be nullified if one attempts to modify Kuroda with multiplexing arrangements for parallel readout, either of one bit simultaneously from each column or of one bit simultaneously from each memory circuit of a block in a column. This latter would be exactly what the Examiner proposes to do, namely taking a known multiplexing arrangement from Clemons and used in this prior art SRAM device dating from 1984 to achieve a bytewise organization in the ferroelectric memory disclosed by Kuroda. Indeed the Examiner has to go further as components such as the Y-SELECT blocks and their WRC circuits now have to be removed from Kuroda and replaced by the multiplexer arrangement of Clemons. But the Examiner gives no hint whether spares are now to be included in Kuroda also. This would indeed have been a sensible move since the proposed hypothetical memory circuit with the multiplexing arrangement of Clemons would have an increased voltage disturb coefficient and lowered reliability.

Hence the prior art ferroelectric memory of Kuroda might be modified by the multiplexer arrangement of Clemons to yield a bytewise parallel read and write, but at the price of throwing out both the selector blocks and the write/read control circuits of Kuroda and ending up with a ferroelectric memory with about the same integration factor, but unfortunately with an eightfold increased voltage disturb coefficient. A person skilled in the art contemplating the teachings of Kuroda could not be led to the hypothetical memory circuit suggested by the Examiner as the resulting memory circuit would not fulfill its objectives. With a much higher voltage disturb coefficient it would not be suited for the applications envisaged by Kuroda which presupposes a very high reliability memory circuit. In this connection note that FEM (ferroelectric memories) are non-volatile as opposed to the

SRAM, also in the sense that they retain the stored datum in case of a power loss. This would not be the case of an SRAM.

Since Clemons is not at all concerned with ferroelectric or electret memories, but rather a semiconductor SRAM memory, it is a dubious claim that Clemons teachings can be hoisted on Kuroda. The teaching of Clemons would actually ruin the expressed object of Kuroda as it would demand that all 8 memory circuits of a block in Kuroda's memory should be selected and connected, for example, a write or read operation. This would increase the voltage stress ratio of Kuroda's memory eightfold, but in addition it would also serve to make Kuroda's memory rather more complicated as it would need a complete rearrangement of the Y-Select block as well as the Write/Read Control Block(WRC). The latter must for instance be equipped with 8 sense amplifiers, but even this would not transform Kuroda's device into one similar of the present invention, with regard to operational features, as further multiplexing arrangements would be needed if for instance the Write/Read Control Blocks were to be conflated into one and used for all columns of this memory. However, it is quite clear that at least what could be termed multiplexing arrangement of Clemons cannot be adapted to a memory of Kuroda in that sense, even when the fact that they are completely different memories are overlooked.

It seems wholly illogical by the standards of one of ordinary skill to transfer structural and operational details of the semiconductor SRAM of Clemons to the active matrix-addressable ferroelectric memory of Kuroda and certainly such an undertaking would not yield the present invention, which specifically is concerned with both limiting the number of sense amplifiers and obtaining a suitable high data rate by an appropriate segmenting of a word line and providing for reading each word line segment in parallel by using a sense amplifier block with the number of sense amplifiers equal to the number of bit lines defining a word line segment in order that a high data rate may be maintained and the number of sense amplifiers kept to manageable proportions, whereas the number of bit lines of the memory according to the present invention can be as large as desired.

Thus, Kuroda in combination with Clemons fails to teach, *inter alia,* each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment, as recited in claims 1, 12 and 13.

Appellant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness. Thus, Appellant maintains that claims 1, 12 and 13 are allowable over the combination of *Kuroda* and *Clemons* for at least the reason noted above.

VIII. CLAIMS

A copy of the claims involved in the present Appeal are attached hereto as Appendix A.

IX. EVIDENCE

There is no additional evidence pursuant to §§ 1.130, 1.131, or 1.132 and/or evidence entered by or relied upon by the examiner that is relevant to this appeal as noted in Appendix B.

X. RELATED PROCEEDINGS

There is no related proceedings known to Appellants.

XI. CONCLUSION

The withdrawal of the outstanding rejections and the allowance of claims 1-5 and 12-18 are earnestly solicited.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, and 1.21 that may be required by this paper and to credit any overpayment to Deposit Account No. 02-2448.

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Respectfully submitted,

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/088,913 are as follows:

Claim 1. (Previously Presented)

A non-volatile passive matrix memory device comprising;

an electrically polarizable dielectric memory material exhibiting hysteresis, wherein said memory material is provided sandwiched in a layer between a first set and second set of respective parallel addressing electrodes, wherein the electrodes of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set, the latter constituting bit lines of the memory device,

wherein a memory cell with a capacitor-like structure is defined in the memory material at the crossings between word lines and bit lines, wherein the memory cells of the memory device constitute the elements of a passive matrix, wherein each memory cell can be selectively addressed for a write/read operation via a word line and bit line, where each memory cell is at all times in physical contact with a word line and a bit line,

wherein a write operation to a memory cell takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell, wherein said applied voltage either establishes a determined polarization state in the memory cell or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage larger than the coercive voltage Vc, to the memory cell and detecting at least one electrical parameter of an output current on the bit lines,

wherein the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing means, thus enabling

simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, each sensing means being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line.

Claim 2. (Previously Presented)

A non-volatile passive matrix memory device according to claim 1, wherein simultaneous connection of each bit line of a segment with the associated sensing means during addressing is accomplished by multiplexers.

Claim 3. (Previously Presented)

A non-volatile passive matrix memory device according to claim 2, wherein the number of multiplexers corresponds to the largest number of bit lines defining a segment, each bit line of a segment being connected with a specific multiplexer.

Claim 4. (Previously Presented)

A non-volatile passive matrix memory device according to claim 3, wherein the output of each multiplexer is connected with a single sensing means.

Claim 5. (Previously Presented)

A non-volatile passive matrix memory device according to claim 4, wherein the single sensing means is a sense amplifier.

Claims 6. – 11. (Withdrawn)

Claim 12. (Previously Presented)

A volumetric data storage apparatus comprising:

a plurality of stacked layers, each layer including one non-volatile passive matrix memory device, the non-volatile passive matrix memory device including an electrically polarizable dielectric memory material exhibiting hysteresis, wherein said memory material is provided sandwiched in a layer between a first set and second set of respective parallel addressing electrodes,

wherein the electrodes of the first set constitute word lines of the memory device and are provided in substantially orthogonal relationship to the electrodes of the second set, the latter constituting bit lines of the memory device,

wherein a memory cell with a capacitor-like structure is defined in the memory material at the crossings between word lines and bit lines,

wherein the memory cells of the memory device constitute the elements of a passive matrix, wherein each memory cell can be selectively addressed for a write/read operation via a word line and bit line and where each memory cell is at all times in physical contact with a word line and a bit line, wherein a write operation to a memory cell takes place by establishing a desired polarization state in the cell by means of a voltage being applied to the cell via the respective word line and bit line defining the cell,

wherein said applied voltage either establishes a determined polarization state in the memory cell or is able to switch between the polarization states thereof, and wherein a read operation takes place by applying a voltage smaller than the switching or polarization voltage Vs, to the memory cell and detecting at least one electrical parameter of an output current on the bit lines,

wherein the word lines are divided into a number of segments, each segment including and being defined by a plurality of adjoining bit lines in the matrix, each word line in a segment is differentiated based on the position of the word line within the segment, each word line in the segment being adjoined to a separate bit line, where each separate bit line assigned to a segment is connected with an a different associated sensing means, such that a word line of the same position within each segment is selected within each segment, each word line of the same

position being sensed at the same time be said respective different associated sensing means, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment for readout via the corresponding bit lines of the segment, each sensing means being adapted for sensing the charge flow in the bit line connected therewith in order to determine a logical value stored in the memory cell defined by the bit line.

Claim 13. (Previously Presented)

A memory device, comprising:

a first set of electrodes which constitute word lines of the memory device;

a second set of electrodes which constitute bit lines of the memory device, the second set of electrodes being positioned substantially orthogonal to the first set of electrodes, the bit lines being divided into a number of segments;

an electrically polarizable dielectric memory material provided in a layer between the first and second set of electrodes, the electrically polarizable dielectric memory material and the first and second set of electrodes forming a passive matrix memory in which each memory cell can be selectively addressed for a write/read operation and where the memory material is at all times in physical contact with the first and second set of electrodes; and

a number of sensing devices connected to each of a corresponding bit lines within each segment of word lines, where each word line in each segment is differentiated based on the position of the word line within the segment, each word line of each segment being adjoined to a separate bit line, such that a word line of the same position within each segment is selected within each segment, each word line of the same position being sensed at the same time by said respective different associated sensing device from the number of sensing devices, thus enabling simultaneous connection of all memory cells assigned to a word line on a segment.

Claim 14. (Previously presented)

A non-volatile passive matrix memory device according to claim 1, wherein the number of sensing means is equal to the number of bit lines within each segment, where each segment

contains the same number of bit lines, such that each bit line in each segment is sensed at a different sensing means.

Claim 15. (Previously presented)

A volumetric data storage apparatus according to claim 12, wherein the number of sensing means is equal to the number of bit lines within each segment, where each segment contains the same number of bit lines, such that each bit line in each segment is sensed at a different sensing means.

Claim 16. (Previously presented)

A memory device according to claim 13, wherein the number of sensing devices is equal to the number of bit lines within each segment, where each segment contains the same number of bit lines, such that each bit line in each segment is sensed at a different sensing device.

Claim 17. (Previously presented)

A non-volatile passive matrix memory device according to claim 1, wherein the electrically polarizable dielectric memory material is ferroelectric material.

Claim 18. (Previously presented)

A volumetric data storage apparatus according to claim 12, wherein the electrically polarizable dielectric memory material is ferroelectric material.

APPENDIX B

There is no additional evidence pursuant to §§ 1.130, 1.131, or 1.132 and/or evidence entered by or relied upon by the examiner that is relevant to this appeal.

APPENDIX C

There are no related proceedings.

APPENDIX D

Additional support material

Table 1;

A1;

B1;

C1-C5; and

D1-D11.